

**Exhibit A to  
Response to Office Action**

**CS152**  
**Computer Architecture and Engineering**

**Lecture 5: Cost and Design**

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**lecture slides:** <http://www-inst.eecs.berkeley.edu/~cs152/>

cs 152 L5 Cost.1

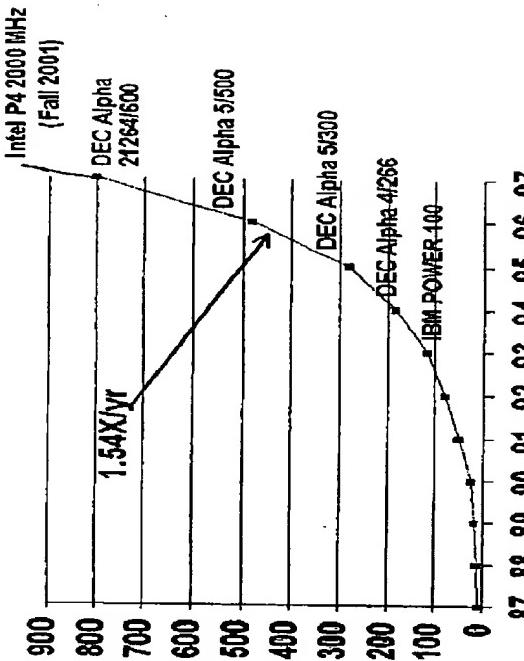
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## Review: Performance and Technology Trends

◦ Technology Power:  $1.2 \times 1.2 \times 1.2 = 1.7 \times / \text{year}$

- Feature Size: shrinks 10% / yr. => Switching speed improves 1.2 / yr.
- Density: improves 1.2x / yr.
- Die Area: 1.2x / yr.

### Technology Trends: Processor Performance



- The lesson of RISC is to keep the ISA as simple as possible:
- Shorter design cycle => fully exploit the advancing technology (~3yr)
- Advanced branch prediction and pipeline techniques
- Bigger and more sophisticated on-chip caches

Processor performance increase/year,  
referred to as Moore's Law (transistors/chip)



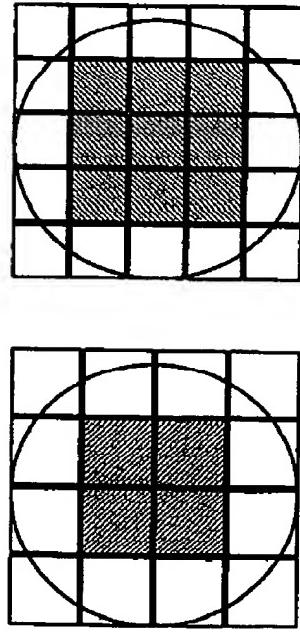
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## Integrated Circuit Costs

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$$\text{Die cost} = \frac{\text{Wafer cost}}{\text{Dies per Wafer} * \text{Die yield}}$$

$$\text{Dies per wafer} \sim \frac{\text{eff Wafer Area}}{\text{Die Area}}$$



$$\text{Die Yield} = \frac{\{ 1 + \frac{\text{Defects_per_unit_area} * \text{Die_Area}}{\text{Wafer yield}} \}}{?}$$

*Die Cost is goes roughly with the cube of the area.*

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